WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory comprising:

first cell units each comprising one memory cell and two select gate transistors between which the memory cell is held;

a word line connected in common to each memory cell of the first cell units;

bit lines individually connected to the first cell units;

sense amplifiers disposed for the bit lines; and

an erase circuit which divides the first cell units into blocks and which sets potentials of the bit lines by a block unit at an erase time.

2. The nonvolatile semiconductor memory according to claim 1, wherein each of the blocks comprises two or more first cell units.

3. The nonvolatile semiconductor memory according to claim 1, wherein each of the blocks includes the first cell units for one byte.

4. The nonvolatile semiconductor memory according to claim 1, wherein at the erase time, data is erased by the block unit.

5. The nonvolatile semiconductor memory according to claim 1, wherein at a data renewal time, data is erased with respect to at least one block which is a renewal object and data program is executed with respect to at least one block.

6. The nonvolatile semiconductor memory according to claim 1, wherein at a data renewal time, the data is erased with respect to all the blocks and data program is executed with respect to all the blocks.

7. The nonvolatile semiconductor memory according to claim 1, wherein the erase circuit comprises high withstand pressure transistors which supply an erase potential to the bit lines, and the high withstand pressure transistors in the same block are controlled by the same column selection signal.

8. The nonvolatile semiconductor memory according to claim 7, wherein the high withstand pressure transistor which can bear the erase potential is connected between the bit lines and sense amplifiers.

9. The nonvolatile semiconductor memory according to claim 1, wherein wells are disposed for the blocks, and the first cell units are disposed in the same well by the block unit.

10. The nonvolatile semiconductor memory according to claim 1, wherein at the erase time, the data erase comprises: generating a high electric field between a drain region and control gate electrode of the memory cell which is an erase object; and extracting electrons into the drain region from a floating gate electrode.

11. The nonvolatile semiconductor memory according to claim 10, wherein the data is erased by hot hole injection into the floating gate electrode from the

drain region.

12. The nonvolatile semiconductor memory according to claim 10, wherein the data erase comprises: extracting electrons into the drain region from the floating gate electrode; and performing hot hole injection into the floating gate electrode from the drain region.

13. The nonvolatile semiconductor memory according to claim 1, wherein data write comprises: generating a high electric field between a channel region and control gate electrode of the memory cell which is a write object; and injecting electrons into a floating gate electrode from the channel region.

14. The nonvolatile semiconductor memory according to claim 1, wherein each memory cell in the first cell units stores the data of one bit or more.

15. The nonvolatile semiconductor memory according to claim 1, further comprising:

second cell units including one or more memory cells; and

one or more word lines connected in common to the second cell units,

wherein the second cell units are individually connected to the bit lines.

16. The nonvolatile semiconductor memory according to claim 15, wherein the number of memory cells included in each of the second cell units is equal to

that of word lines connected to the second cell units.

17. The nonvolatile semiconductor memory according to claim 15, wherein the second cell unit is an NAND cell unit in which memory cells are connected in series.

18. The nonvolatile semiconductor memory according to claim 15, wherein the second cell unit is an AND cell unit or a DINOR cell unit in which memory cells are connected in parallel.

19. The nonvolatile semiconductor memory according to claim 15, wherein the second cell unit is an NOR cell unit comprising one memory cell and one select gate transistor.

20. A nonvolatile semiconductor memory comprising:

first cell units each comprising one memory cell and two select gate transistors between which the memory cell is held;

a word line connected in common to each memory cell of the first cell units;

bit lines individually connected to the first cell units;

sense amplifiers disposed for the bit lines;

source lines which divide the first cell units into blocks and which are connected to the first cell units; and

an erase circuit which sets potentials of the source lines by a block unit at an erase time.

21. The nonvolatile semiconductor memory according to claim 20, wherein each of the blocks comprises two or more first cell units.

22. The nonvolatile semiconductor memory according to claim 20, wherein each of the blocks includes the first cell units for one byte.

23. The nonvolatile semiconductor memory according to claim 20, wherein at the erase time, data is erased by the block unit.

24. The nonvolatile semiconductor memory according to claim 20, wherein at a data renewal time, data is erased with respect to at least one block which is a renewal object and data program is executed with respect to at least one block.

25. The nonvolatile semiconductor memory according to claim 20, wherein at a data renewal time, the data is erased with respect to all the blocks and data program is executed with respect to all the blocks.

26. The nonvolatile semiconductor memory according to claim 20, wherein the erase circuit comprises high withstand pressure transistors which supply an erase potential to the source lines, and the high withstand pressure transistors in the same block are controlled by the same column selection signal.

27. The nonvolatile semiconductor memory according to claim 20, wherein wells are disposed for the blocks, and the first cell units are disposed in the same well

by the block unit.

28. The nonvolatile semiconductor memory according to claim 20, wherein at the erase time, the data erase comprises: generating a high electric field between a source region and control gate electrode of the memory cell which is an erase object; and extracting electrons into the source region from a floating gate electrode.

29. The nonvolatile semiconductor memory according to claim 28, wherein the data is erased by hot hole injection into the floating gate electrode from the source region.

30. The nonvolatile semiconductor memory according to claim 28, wherein the data erase comprises: extracting electrons into the source region from the floating gate electrode; and performing hot hole injection into the floating gate electrode from the source region.

31. The nonvolatile semiconductor memory according to claim 20, wherein data write comprises: generating a high electric field between a channel region and control gate electrode of the memory cell which is a write object; and injecting electrons into a floating gate electrode from the channel region.

32. The nonvolatile semiconductor memory according to claim 20, wherein each memory cell in the first cell units stores the data of one bit or more.

33. The nonvolatile semiconductor memory according

to claim 20, further comprising:

second cell units including one or more memory cells; and

one or more word lines connected in common to the second cell units,

wherein the second cell units are individually connected to the bit lines.

34. The nonvolatile semiconductor memory according to claim 33, wherein the number of memory cells included in each of the second cell units is equal to that of word lines connected to the second cell units.

35. The nonvolatile semiconductor memory according to claim 33, wherein the second cell unit is an NAND cell unit in which memory cells are connected in series.

36. The nonvolatile semiconductor memory according to claim 33, wherein the second cell unit is an AND cell unit or a DINOR cell unit in which memory cells are connected in parallel.

37. The nonvolatile semiconductor memory according to claim 33, wherein the second cell unit is an NOR cell unit comprising one memory cell and one select gate transistor.

38. A nonvolatile semiconductor memory comprising:

first cell units each comprising memory cells connected in series and two select gate transistors between which the memory cells are held;

second cell units each comprising one memory cell and one select gate transistor;

bit lines which are individually connected to the first cell units and which are individually connected to the second cell units and which are connected in common to the first and second cell units; and

sense amplifiers disposed for the bit lines,

wherein at least an FN tunnel current is used with respect to the respective memory cells in the first and second cell units to perform write/erase.

39. The nonvolatile semiconductor memory according to claim 38, further comprising:

an erase circuit which divides the first and second cell units into blocks and which sets potentials of the bit lines by a block unit at an erase time.

40. The nonvolatile semiconductor memory according to claim 38, further comprising:

source lines which divide the first and second cell units into blocks and which are connected in common to the first and second cell units; and

an erase circuit which sets potentials of the source lines by a block unit at an erase time.

41. A memory chip comprising the nonvolatile semiconductor memory according to claim 1, 20, 33, or 38.

42. A memory chip comprising:

the nonvolatile semiconductor memory according to claim 1, 20, 33, or 38; and

a logic circuit which controls the nonvolatile semiconductor memory.

43. The memory chip according to claim 42, wherein the logic circuit is a CPU.

44. A memory card comprising: the memory chip according to claim 41, 42, or 43.

45. A memory card comprising:

the memory chip according to claim 41, 42, or 43; and

a controller which controls the memory chip.

46. A memory card system comprising:

a memory card including the memory chip according to claim 41, 42, or 43; and

an electronic machine which is inserted in the memory card.

47. A data renewal method in which a nonvolatile semiconductor memory is used as an object, the memory comprising: cell units each including one memory cell and two select gate transistors holding the memory cell between them; a word line connected in common to the memory cells of the cell units; and bit lines individually connected to the cell units, the method comprising:

performing data erase with respect to only the respective memory cells in the cell unit which is a renewal object in the cell units; and

thereafter performing data write with respect to

only the respective memory cells in the cell unit which is the renewal object.

48. The data renewal method according to claim 47, wherein the data erase comprises: generating a high electric field between a drain region and control gate electrode of each memory cell in the cell unit which is the renewal object; and extracting electrons into the drain region from a floating gate electrode.

49. The data renewal method according to claim 48, wherein the data erase comprises: performing hot hole injection into the floating gate electrode from the drain region.

50. The data renewal method according to claim 48, wherein the data erase comprises: extracting electrons into the drain region from the floating gate electrode; and performing hot hole injection into the floating gate electrode from the drain region.

51. The data renewal method according to claim 47, wherein the data erase comprises: generating a high electric field between a source region and control gate electrode of each memory cell in the cell unit which is the renewal object; and extracting electrons into the source region from a floating gate electrode.

52. The data renewal method according to claim 51, wherein the data erase comprises: performing hot hole injection into the floating gate electrode from the source region.

53. The data renewal method according to claim 51, wherein the data erase comprises: extracting electrons into the source region from the floating gate electrode; and performing hot hole injection into the floating gate electrode from the source region.

54. The data renewal method according to claim 47, wherein the data erase is performed by the byte unit based on a column selection signal.

55. The data renewal method according to claim 47, further comprising: selecting one of a mode which is executed by a byte unit and a mode which is executed by a page unit at the data erase time.

56. The data renewal method according to claim 47, wherein the data write comprises: generating a high electric field between a channel region and control gate electrode of each memory cell in the cell unit which is a write object in the cell units which are the renewal objects; and injecting electrons into a floating gate electrode from the channel region.

57. The data renewal method according to claim 56, wherein the high electric field is not generated between the channel region and control gate electrode of each memory cell in the cell unit which is not the renewal object and of each memory cell in the cell unit which is not the write object in the cell units which are the renewal objects.

58. A data erase method with respect to a cell

unit comprising a first select gate transistor in which a drain region is connected to the bit line, a second select gate transistor in which a source region is connected to a source line, and a memory cell which is connected between the first and second select gate transistors and which comprises a control gate electrode and floating gate electrode, the method comprising:

supplying a first potential to the bit line, supplying a second potential higher than the first potential to the gate electrode of the first select gate transistor, and supplying a third potential lower than the first potential to the control gate electrode; and

extracting electrons to the drain region from the floating gate electrode to erase data of the memory cell.

59. The data erase method according to claim 58, wherein the first and second potentials are positive potentials, and the third potential is a ground potential.

60. The data erase method according to claim 59, further comprising: supplying the positive potential to a gate electrode of the second select gate transistor; supplying a negative potential to the source line; extracting electrons into the drain region from the floating gate electrode; and injecting hot holes into

the floating gate electrode from the drain region to erase the data of the memory cell.

61. The data erase method according to claim 59, further comprising: supplying the positive potential to a well region in which the memory cell and the first and second select gate transistors are formed; extracting electrons into the drain region from the floating gate electrode; and injecting hot holes into the floating gate electrode from the drain region to erase the data of the memory cell.

62. The data erase method according to claim 58, wherein the first and second potentials are positive potentials, and the third potential is a negative potential.

63. The data erase method according to claim 62, further comprising: supplying the positive potential to a gate region of the second select gate transistor; supplying the negative potential to the source line; extracting electrons into the drain region from the floating gate electrode; and injecting hot holes into the floating gate electrode from the drain region to erase the data of the memory cell.

64. The data erase method according to claim 62, further comprising: supplying the positive potential to a well region in which the memory cell and the first and second select gate transistors are formed; extracting electrons into the drain region from the

floating gate electrode; and injecting hot holes into the floating gate electrode from the drain region to erase the data of the memory cell.

65. A data erase method with respect to a cell unit comprising a first select gate transistor in which a drain region is connected to a bit line, a second select gate transistor in which a source region is connected to the source line, and a memory cell which is connected between the first and second select gate transistors and which comprises a control gate electrode and floating gate electrode, the method comprising:

supplying a first potential to the source line, supplying a second potential higher than the first potential to the gate electrode of the second select gate transistor, and supplying a third potential lower than the first potential to the control gate electrode; and

extracting electrons into the source region from the floating gate electrode to erase data of the memory cell.

66. The data erase method according to claim 65, wherein the first and second potentials are positive potentials, and the third potential is a ground potential.

67. The data erase method according to claim 66, further comprising: supplying the positive potential to

a gate electrode of the first select gate transistor; supplying a negative potential to the bit line; extracting electrons into the source region from the floating gate electrode; and injecting hot holes into the floating gate electrode from the source region to erase the data of the memory cell.

68. The data erase method according to claim 66, further comprising: supplying the positive potential to a well region in which the memory cell and the first and second select gate transistors are formed; extracting electrons into the source region from the floating gate electrode; and injecting hot holes into the floating gate electrode from the source region to erase the data of the memory cell.

69. The data erase method according to claim 65, wherein the first and second potentials are positive potentials, and the third potential is a negative potential.

70. The data erase method according to claim 69, further comprising: supplying the positive potential to a gate region of the second select gate transistor; supplying the negative potential to the source line; extracting electrons into the drain region from the floating gate electrode; and injecting hot holes into the floating gate electrode from the drain region to erase the data of the memory cell.

71. The data erase method according to claim 69,

further comprising: supplying the positive potential to a well region in which the memory cell and the first and second select gate transistors are formed; extracting electrons into the drain region from the floating gate electrode; and injecting hot holes into the floating gate electrode from the drain region to erase the data of the memory cell.

72. An embedded memory chip comprising:

at least two memory cell arrays of different types,

wherein the at least two memory cell arrays comprises at least two of:

a first memory cell array including a first cell unit constituted of one memory cell and one select gate transistor;

a second memory cell array including a second cell unit constituted of one memory cell and two select gate transistors between which the memory cell is held; and

a third memory cell array including a third cell unit constituted of memory cells.

73. The embedded memory chip according to claim 72, wherein each of the memory cells in the first to third cell units includes a stacked gate structure including a floating gate electrode and control gate electrode.

74. The embedded memory chip according to claim 73, wherein each of the memory cells in the first

to third cell units uses an FN tunnel phenomenon to perform data write/erase.

75. The embedded memory chip according to claim 72, wherein the third cell unit is a NAND cell unit in which the memory cells are connected in series, or an AND cell unit or DINOR cell unit in which the memory cells are connected in parallel.

76. The embedded memory chip according to claim 72, wherein the at least two memory cell arrays are disposed independent of each other.

77. The embedded memory chip according to claim 72, wherein the at least two memory cell arrays are disposed adjacent to each other, and share the bit line.

78. The embedded memory chip according to claim 77, wherein the at least two memory cell arrays share a circuit for write and read.

79. The embedded memory chip according to claim 72, further comprising:

a control circuit which reads page data into a sense amplifier circuit with respect to the at least two memory cell arrays and which overwrites the data by a byte unit in the sense amplifier circuit and performs page-erase and which performs page-write of the data of the sense amplifier circuit to renew the data by the byte unit.

80. The embedded memory chip according to

claim 72, further comprising:

a control circuit which reads page data into a sense amplifier circuit with respect to the at least two memory cell arrays and which overwrites the data by a byte unit in the sense amplifier circuit and performs page-erase and which performs page-write of the data of the sense amplifier circuit to renew the data by the byte unit.

81. The embedded memory chip according to claim 72, further comprising:

a control circuit which reads byte data into a sense amplifier circuit with respect to the at least two memory cell arrays and which overwrites the data by a byte unit in the sense amplifier circuit and performs byte-erase and which performs byte-write of the data of the sense amplifier circuit to renew the data by the byte unit.

82. The embedded memory chip according to claim 72, further comprising:

a control circuit which latches byte data as write data in a sense amplifier circuit with respect to the at least two memory cell arrays and performs byte-erase and which performs byte-write of the data of the sense amplifier circuit to renew the data by the byte unit.

83. The embedded memory chip according to claim 72, further comprising: a logic circuit.

84. The embedded memory chip according to

claim 72, further comprising: a logic circuit; and an RF circuit.

85. A memory card comprising: the embedded memory chip according to claim 72.

86. A memory card comprising:

the embedded memory chip according to claim 72; and

a controller which controls the embedded memory chip.

87. A memory card system comprising:

a memory card including the embedded memory chip according to claim 72; and

an electronic machine which is inserted in the memory card.